Paper No. 31

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EISAKU SAIKI, SHINTARO SUZUMURA, TERUMI TAKASHI, KAZUTOSHI ASHIKAWA, TSUGUYOSHI HIROOKA, SHOICHI MIYAZAWA and MASASHI MORI,

Appeal No. 2000-0373
Application No. 08/450,245

HEARD: January 17, 2002

Before KRASS, BARRETT and BARRY, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-4, 7 and 18-23. Claims 5, 6 and 8-17 have been withdrawn as being directed to a nonelected invention.

The invention is directed to a magnetic recording and reproducing apparatus. Appellants discovered that there is a problem when a group of serial write data is

transmitted from a read/write signal processor to a read/write amplifier because the data transmission rate between the two circuits is unacceptably low and does not match the processing capabilities of other components within the system. More specifically, appellants discovered that this low transmission capability is due to the inexpensive film cable typically connecting the two circuits. Appellants' solution is to employ a read/write signal processor having an interleave write data generator for generating a plurality of interleave write data in an interleave relation with each other from write data, whereby each of the plurality of interleave write data is transmitted from the read/write signal processor to the read/write amplifier by using a plurality of signal lines. The read/write amplifier has a compound circuit for restoring, i.e., interleave-to-serial converting, the plurality of interleave write data back into the original, serial, write data.

Representative independent claim 1 is reproduced as follows:

> 1. A magnetic recording and reproducing apparatus transmitting data between a read/write signal processor and a read/write amplifier, for recording and reproducing the data to and from a magnetic recording medium through the read/write amplifier, comprising:
>
> a read/write signal processor having an interleave write data generator for generating a plurality of interleave write data in an interleave relation with each other from write data; and
>
> a read/write amplifier having a compound circuit for restoring the

plurality of interleave write data into original write data;

wherein the read/write signal processor is connected to the read/write amplifier by a plurality of signal lines, whereby each of the plurality of interleave write data is transmitted from the read/write signal processor to the read/write amplifier by using the plurality of signal lines.

The examiner relies on the following references:

Precourt	4,000,513	Dec. 28, 1976
Galbraith et al. (Galbraith)	4,964,107	Oct. 16, 1990
Noguchi et al. (Noguchi)	5,355,263	Oct. 11, 1994
Behrens et al. (Behrens)	5,359,631	Oct. 25, 1994
Kondo	5,481,554	Jan. 02, 1996
Shrinkle	5,530,600	Jun. 25, 1996

Claims 1-4, 7 and 18-23 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites Noguchi and Kondo with regard to claims 1, 18-20, 22 and 23, adding Galbraith with regard to claim 2. The examiner cites Precourt and Behrens with regard to claim 3, adding Galbraith with regard to claims 4 and 21. With regard to claim 7, the examiner cites Noguchi, Kondo and Shrinkle.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We will reverse as to the rejections relying on Noguchi and Kondo, in whole or in part, as we do not find that the examiner has established a prima facie case of

obviousness with regard to the instant claimed subject matter. However, we will sustain the rejections of claims 3, 4 and 21, under 35 U.S.C. § 103, relying on the combination of Precourt and Behrens, either in whole or in part.

In applying Noguchi to instant claim 1, the examiner contends that Noguchi teaches a read/write processor 25 having an interleave write data generator, citing column 2, lines 47-49, a read/write amplifier 27 and a compound circuit, identifying column 2, lines 49-50. The examiner interprets the parallel-serial converter as being the claimed "compound circuit" because it restores the interleave data to its original form. The trouble here is that Noguchi's parallel/serial converter is not part of the amplifier. While the examiner recognizes this, the examiner contends that the parallel/serial converter is connected to the input of the amplifier and, so, is "functionally equivalent to being a part of the amplifier" [answer-page 3].

The examiner also recognizes that Noguchi fails to teach the read/write signal processor being connected to the read/write amplifier by a plurality of lines. Thus, the examiner turns to Kondo, wherein a signal processor 12 is connected to the amplifier 13 by a plurality of lines, whereby the plurality of interleaved write data is transmitted between the amplifier and the signal processor by the plurality of lines, referring to Figure 1B. The examiner then concludes that it would have been obvious to modify the

teachings of Noguchi to include the teachings of Kondo, the "motivation being to provide a data transmitting apparatus which can correct errors as set forth in col. 2, lines 34-47 of Kondo" [answer-page 4].

We agree with appellants that the examiner appears to be relying on impermissible hindsight in reaching the conclusion of obviousness of the claimed subject matter.

Noguchi and Kondo do describe the interleaving of data. However, as explained by appellants, at page 8 of the principal brief, Noguchi's interleaving circuit is at a different location and used for a different purpose than appellants'. Noguchi employs the interleaving circuit for storing and retrieving input audio data between signal processor 25 and memory 26. It would also appear that Noguchi uses a serial, single data signal line, rather than a plurality of lines, between the signal processor 25 and the recording heads.

Kondo's head interleave circuit 12 generates six channels of record data and supplies each channel of the record data through a respective recording amplifier 13, to a respective one of six heads H1-H6. Kondo's arrangement is directed to making error correction easier.

The question becomes, what would have led the skilled artisan, from these somewhat disparate teachings, to have looked to the error correction circuitry of Kondo for

any suggestion as to modifying anything in Noguchi? Noguchi has error correction circuitry [column 2, lines 47-50], and there is no indication that there is any problem therewith. Therefore, there would have been no reason for the artisan to look to add an error correction circuit to Noguchi.

The examiner contends that it would have been obvious to employ alternative error correction circuits. However, we agree with appellants that Noguchi provides the error correction circuitry at the input/output of memory 26 in order to prevent errors in the memory operation. In Kondo, block code data is transmitted and used to correct errors that might be present in quantized data. We are at a loss to see why, without guidance from appellants' disclosure, the artisan would have eliminated the error correction circuitry from the input/output of Noguchi's memory and placed it elsewhere in the system, as disclosed by Kondo.

Moreover, even if the artisan would have been led, in some manner, to do so, it is still not clear to us how one arrives at the instant claimed subject matter.

Claim 1 calls for a very specific combination of elements and interrelated functions. The signal processor has the interleave write data and the amplifier has the

circuit for restoring the interleave data. The processor and the amplifier are interconnected by a plurality of signal lines and each of the plurality of interleave write data

is transmitted from the signal processor to the amplifier by using the plurality of signal lines. Yet, we find nothing in the combination of Noguchi/Kondo which restores the plurality of interleave write data into the original write data wherein the signal processor and the restoring amplifier are interconnected by a plurality of signal lines.

The examiner contends that Noguchi teaches the restoring of the interleave data into original data (column 2, lines 48-50) and that Kondo teaches a plurality of interleaved write data being transmitted between the amplifier and the signal processor. But, even assuming, arguendo, that the examiner's assessment of the references is correct, this still does not answer the question as to why the skilled artisan, without the guidance of appellants' disclosure, would have picked and chosen only certain elements of each reference and arranged them in the specific manner as claimed by appellants.

Accordingly, we will not sustain the rejection of claim 1 under 35 U.S.C. § 103. Similarly, since the arguments are very similar with regard to independent claims 18 and 23, we also will not sustain the rejection of these claims under 35 U.S.C. § 103, or of claims 19, 20 and 22, dependent on the independent claims.

Since Galbraith does not cure the deficiencies of Noguchi and Kondo, we also will not sustain the rejection of claim 2 under 35 U.S.C. § 103 and because Shrinkle does not provide for these deficiencies, we also will not sustain the rejection of claim 7 under 35

U.S.C. § 103.

With regard to independent claim 3, the examiner applies Precourt and Behrens against this claim. More particularly, the examiner contends that Precourt discloses a write signal processor 10, 12 and a write amplifier 16 for recording data, with the write signal processor converting the write data into NRZI and wherein the write data is transmitted between the write amplifier and the write signal processor in the NRZI code. The examiner refers to column 3, lines 40-68 and Figure 1 of Precourt.

Admitting that Precourt does not teach a read/write signal processor and a read/write amplifier, the examiner cites Behrens for such a teaching as well as converting write data into NRZI code, referring to Figure 1 and column 1, lines 28-43 of Behrens.

Finally, the examiner concludes that it would have been obvious to modify Precourt to include the teachings of Behrens because "it is well known in the art to use read/write amplifiers and read/write signal processors" because they "help to simplify the circuit construction, and save time and money" [answer-page 6].

Claim 3 requires that the read/write signal processor have a "conversion circuit for converting the write data into a Non-Return-To-Zero-Interleaved (NRZI) code, whereby the write data is transmitted between the read/write amplifier and the read/write signal processor in the NRZI code."

Clearly, Precourt, as construed by the examiner, discloses an encoder, 10 (which may be considered a signal processor), which converts write data into NRZI code. See column 3, lines 45-48 of Precourt. The signal from encoder 10 is transmitted via compensator 14 to write driver 16 (construed by the examiner as the amplifier). Thus, the issue is whether the NRZI converted write data is still NRZI coded when it reaches the write driver. Appellants contend that the output of Precourt's write delay compensator 14, 24 does not appear to be NRZI code [principal brief-page 17], while the examiner states that while Precourt "mentions a serial to parallel converter in col. 6, lines 23-25, there is no suggestion that the NRZI data has been decoded" [answer-page 10].

Since the examiner makes a reasonable case that Precourt makes no mention of decoding or changing the NRZI signal from encoder 10 in Figure 1, or from shift register 202 in Figure 3, although there is a serial to parallel conversion of the signal, and appellants have offered no evidence to the contrary, except to say that the output

of compensator 14, 24 "does not appear" to be NRZI code, we will find for the examiner on this issue.

While appellants compare instant Figure 3 with Figure 3 of Precourt, contending that, in the former, the input signal to read/write amplifier 2 is NRZI in relation with the interleave write data, thereby reducing the signal frequency therebetween, appellants point

to no claim language directed to such a difference. Accordingly, this argument is not persuasive of patentability.

Appellants base their argument on the presumption that neither Precourt nor Behrens discloses a "conversion circuit..." However, as we find, supra, Precourt does, indeed, disclose such a conversion circuit whereby the write data is transmitted between the amplifier and the signal processor in the NRZI code, appellants' arguments have been answered in full and found not to be persuasive.

Accordingly, we will sustain the rejection of claim 3 under 35 U.S.C. § 103.

We will also sustain the rejection of claims 4 and 21 under 35 U.S.C. § 103 because, as is clear from appellants' "arguments" at page 19 of the principal brief, appellants make the same arguments as with regard to independent claim 3. Thus, claims 4 and 21 will fall with claim 3.

We have sustained the rejection of claims 3, 4 and 21 under 35 U.S.C. § 103 but we have not sustained the rejection of claims 1, 2, 7, 18-20, 22 and 23 under 35 U.S.C. § 103.

Accordingly, the examiner's decision is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may

be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS Administrative Patent Judge	)))
LEE E. BARRETT Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
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